Hardware-Manual of Bio@Fox

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Version 0.13

Contents

Chapter 1

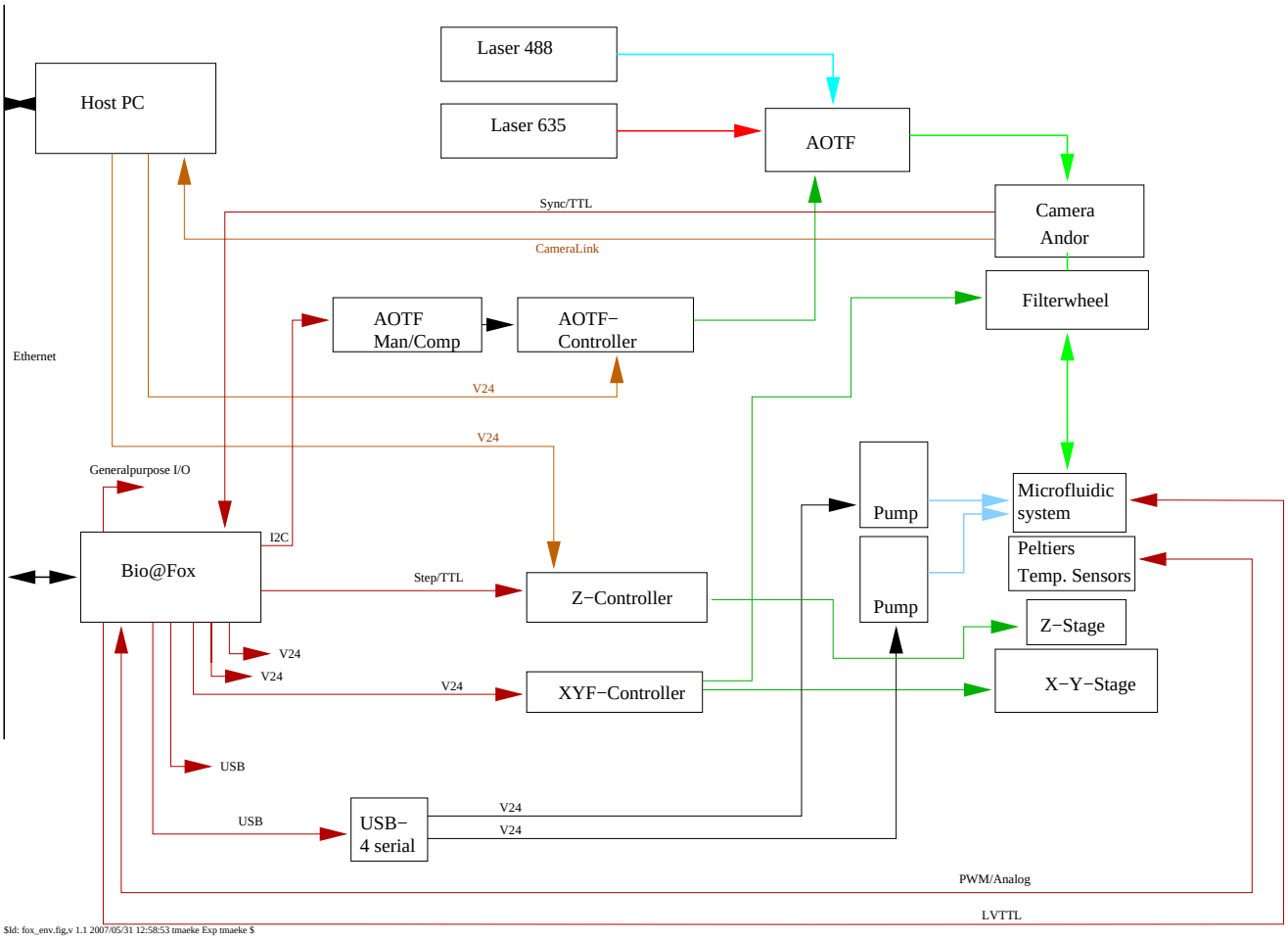
Introduction

This manual is meant for hard- and software-developers working on and with BioMIPs new control device Bio@Fox. It is the central device for connecting to the electronic microfluidic chip and many other devices needed for microfluidic and fluorescent microscopy.

The controller board Bio@Fox is composed of an embedded 100MHz microcontroller pcb (foxboard) running Linux as operating system and an interface pcb with peripherals and converter to connect to the outside equipment.

As main peripheral component the Xilinx FPGA XC3S100E connects to the foxboard and controls most of the other components. It directly connects the microfluidic FPGA, controls the two A/D-converter (UTI03), drives the three optoisolated H-bridges through PWMs, addresses the AOTF-controller via I2C-bus, triggers the Z-stage and can be synchronized by a camera. Thus allows all processes together with the software running in the foxboard acting in realtime. E.g.: at the end of an image aqusition, a camera sync pulse leads to a change of the laser color or intensity and the z-stage can move synchronously. At the same time the electrodes in the microfluidic can pulse and the temperature is performed.

With over 40 individually controllable digital I/O pins with at least five different I/O standards each make this board an ideal and cheap tool for complex system-integration tasks. A programmable Voltage controller allows different Vcc for these pins (1.2V, 1.7V, 1.8V, 2.5V, 3.3V) which offers an alternative peak voltage for the electrodes in the microfluidic.

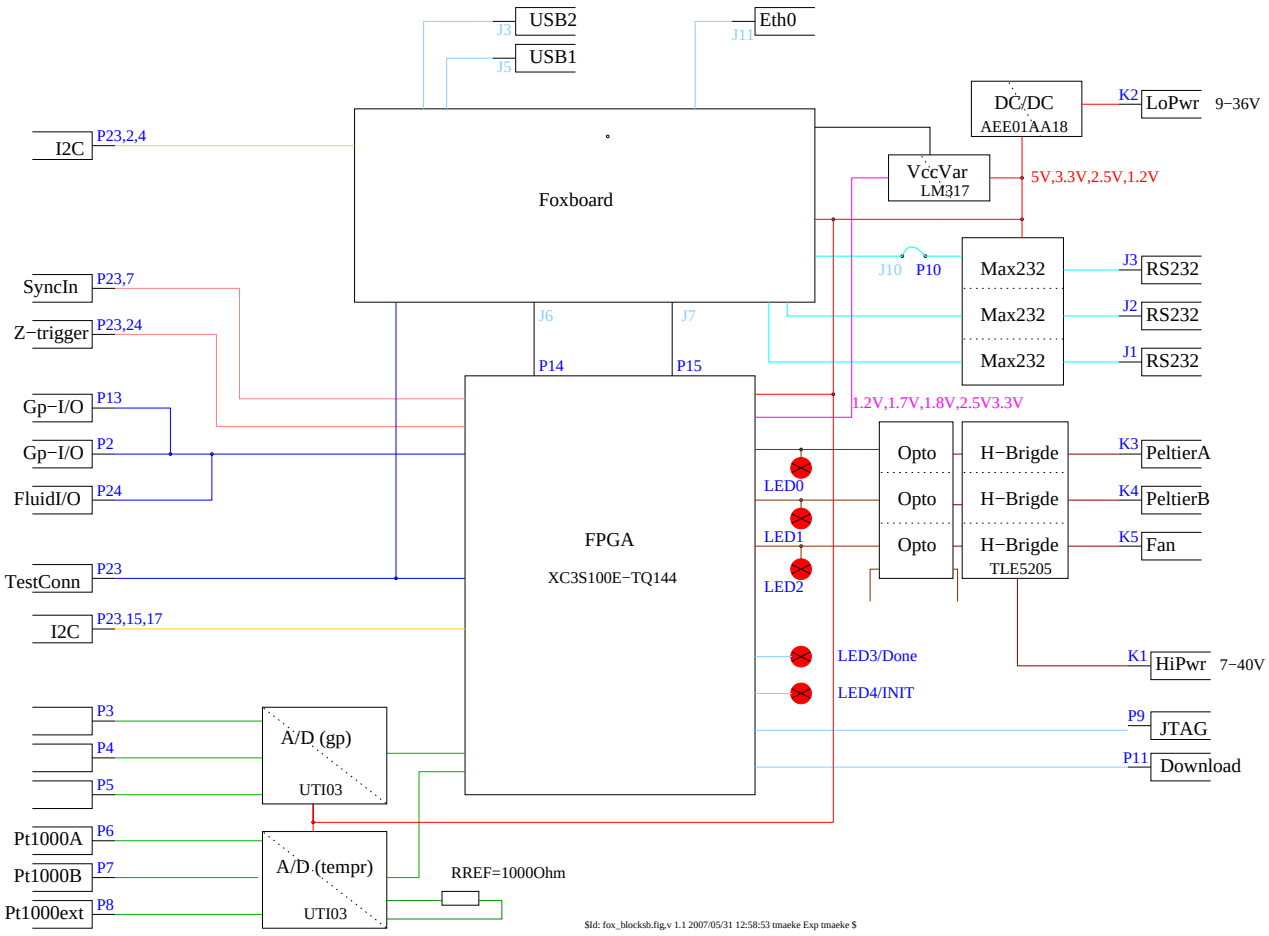


The figure illiustrates how the Bio@Fox device connects other equipment with different interfaces within a microfluidic

and microscopy environment.

Chapter 2

Hardware



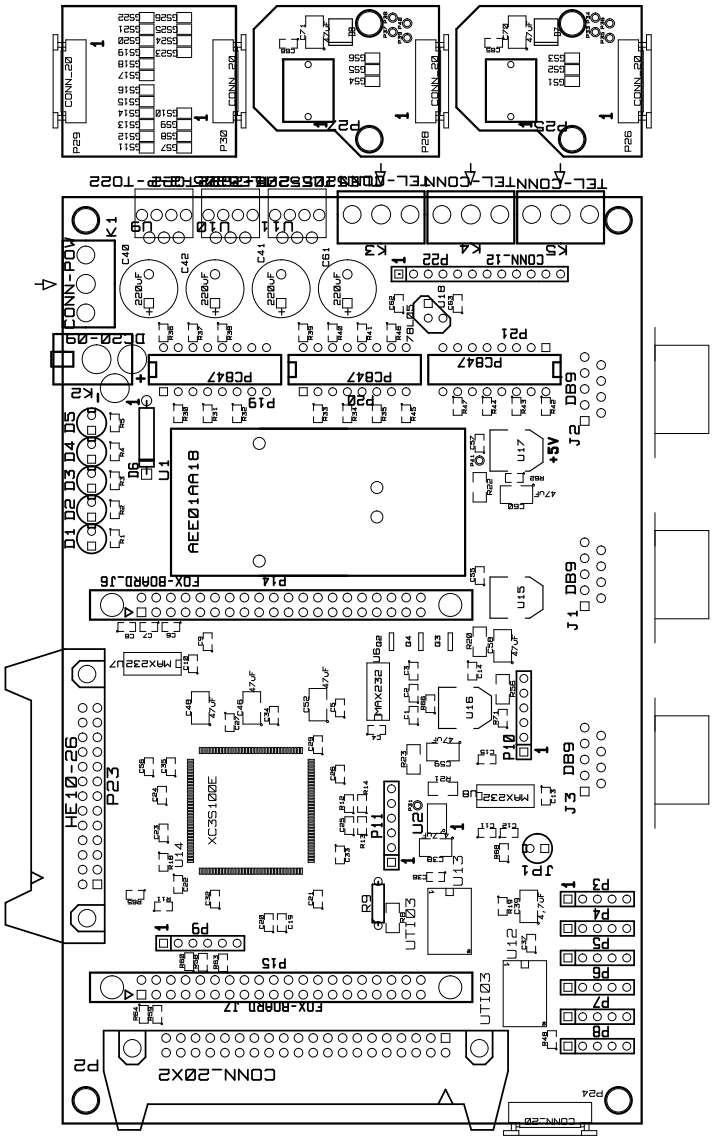
2.1 Interfaces

Interfaces of Bio@Fox:

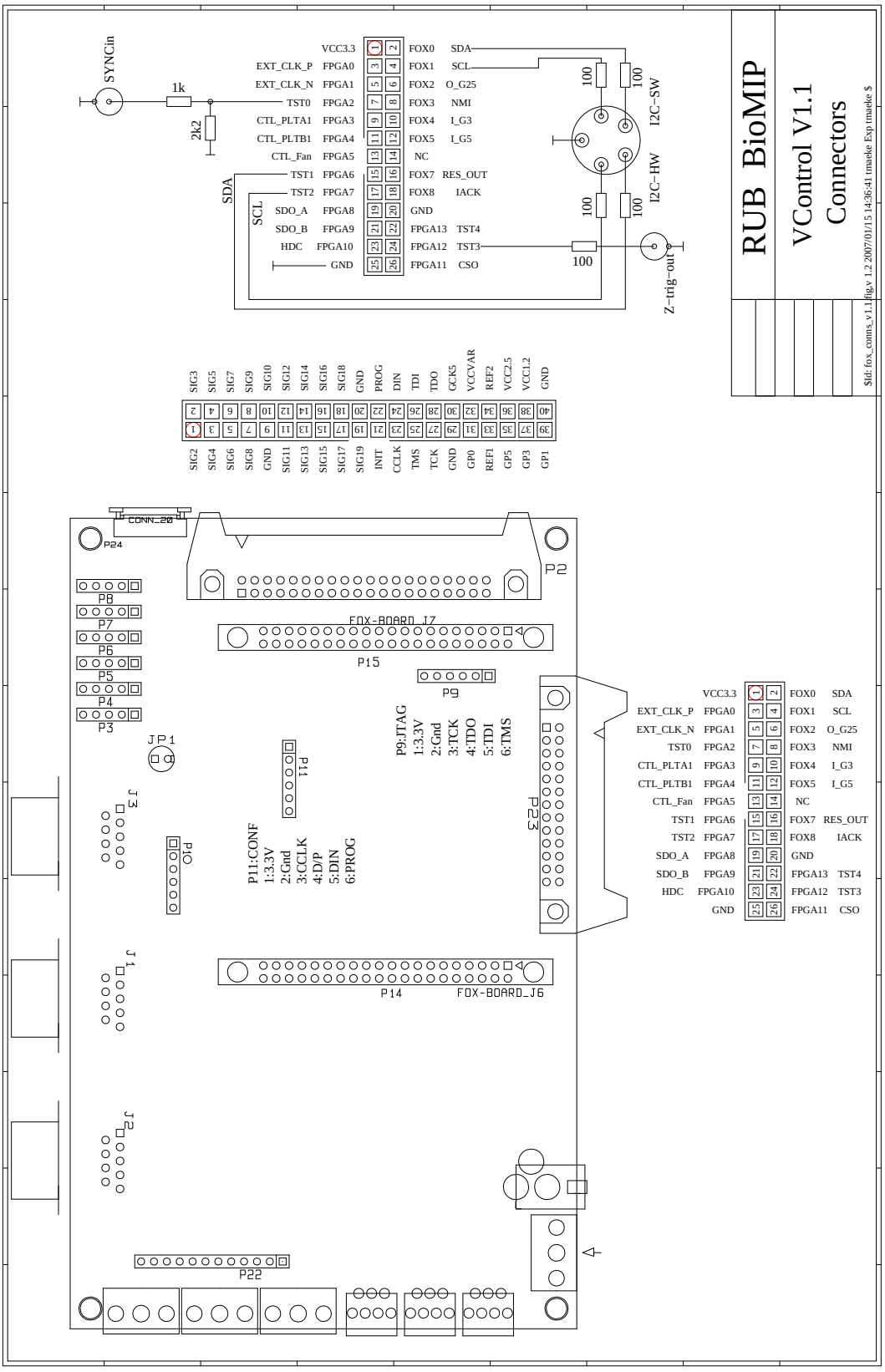
type	no	comment	connector (no of pins)	pcb-id	see
RS-232	3	(foxboard) J3 used as console	DSUB-9	J1,J2,J3	2.3.4
Pt1000	3	internal Reference 1000Ohm	jumper 5 pin	P6,P7,P8	2.1.4
A/D	3	for up to 3 R or 3 C meas.	jumper 5 pin	P3,P4,P5	2.1.3
PWM	3	4A 40V H-bridges	jumper 3 pin	K3,K4,K5	2.1.4
USB	2	(foxboard)	USB type A	foxJ3,foxJ5	2.5.2
Ethernet	1	(foxboard)	RJ-45	foxJ11	2.5.2
I2C	1	Hardware (fast)	jumper 3 pin	P23	2.1.2
I2C	1	Software (slow)	jumper 3 pin	P23	2.1.2
JTAG	1	for FPGA	jumper 7 pin	P9	2.1.3
FPGA	1	for FPGA dowload	jumper 7 pin	P11	2.1.3
Sync In	1	camera sync	1pin	P23	2.1.2
Trigger Out	1	z-stage trigger	1 pin	P23	2.1.2
Opto I/O	1	1 in, 1 out	2 pin	P22	2.3.5
FPFA I/O	1	for microfluidic-FPGA control	20 pin flex	P24	2.3.1
GP I/O	1	includes FPFA pins	40 pin flex/jumper	P2,P13	2.1.2
Test I/O	1	test-pins and internal signals	26 pin jumper	P23	2.1.2

J10 from foxboard directly connects to P10 of the interfaceboard.

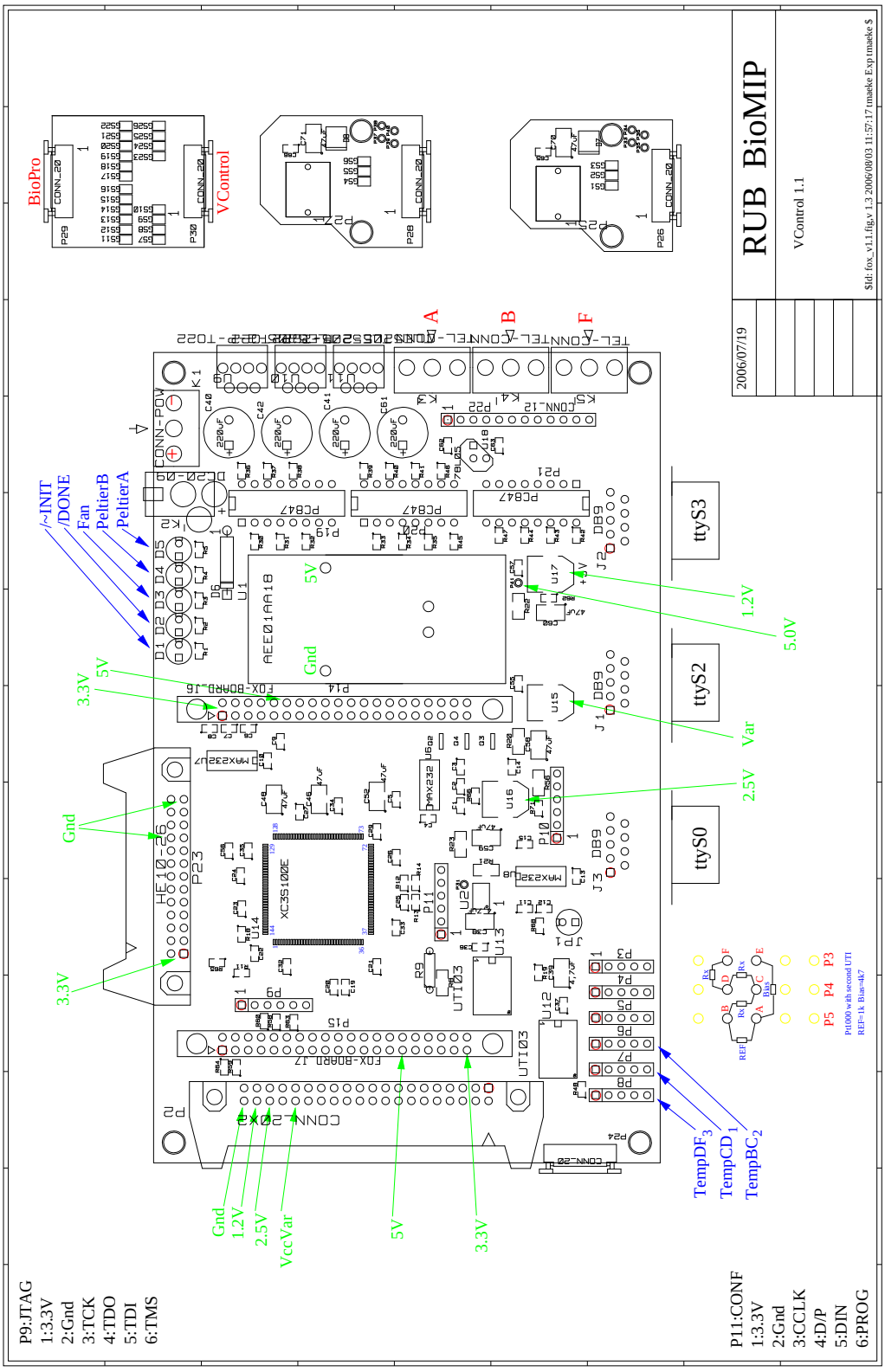
2.1.1 Connector positions



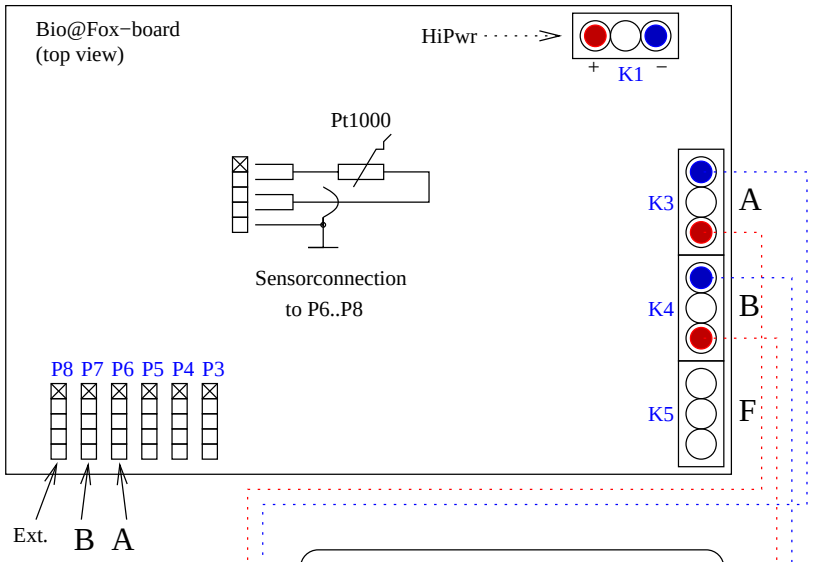
2.1.2 Connector P2, P23

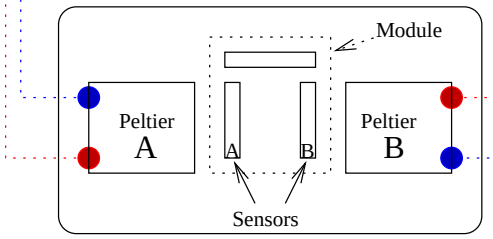


2.1.3 VCC-, Groundpositions, Microfluidic-device-Adapter, P9, P11



2.1.4 Temperature control



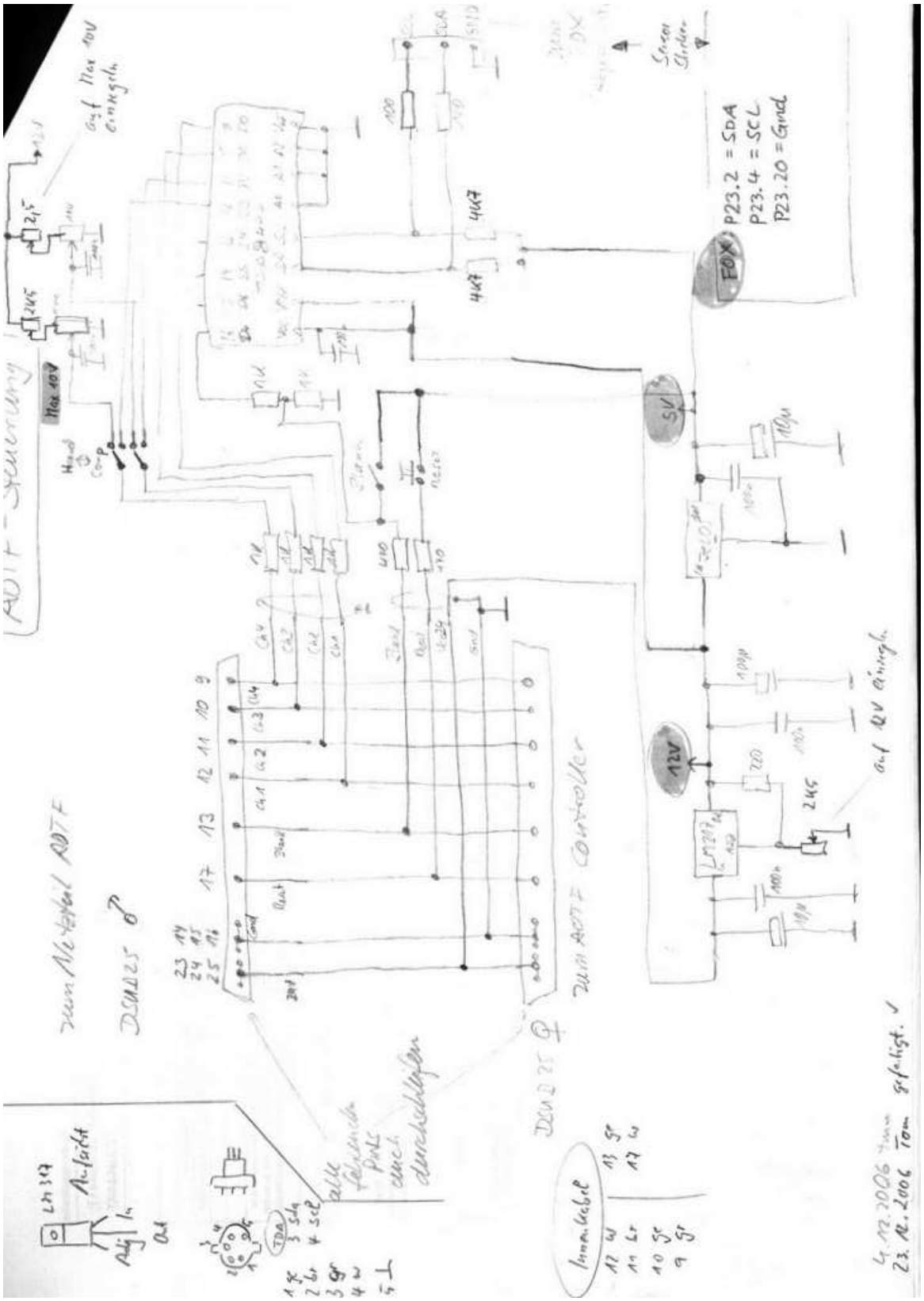


Peltier: TECB−13
Pmax: 18.7W
Imax: 3.9A
Umax: 8.6V
deltaTmax: 71 °C
30x30x4.7mm^3

BioPro modulecarrier

$Id: fox_tempctrl.fig,v 1.1 2007/05/31 12:58:53 tmaeke Exp tmaeke $

2.1.5 Controller for the AOTF controller (preliminary)



2.2 BOM

value	case	references
XC3S100E-TQ144	TQ144	U14

UTI03-SOIC18	SOIC18-WIDE	U12 U13
TLE5205-2-P-TO22	P-TO220-7-11	U9 U10 U11
PC847	16dip300	P19 P20 P21
NPN	SOT23EBC	Q2 Q3 Q4
MAX232	SOIC16	U6 U7 U8
LM317_SOT223	SOT223_LM317	U15 U16 U17
ASFL1_33VDC	CCO_ASFL1	U2
AEE01AA18	AEE01AA18	U1
78L05	TO-92	U18

LED	LEDV	D1 D2 D3 D4 D5
DIODE	DO_213AB	D7 D8
DIODE	D5	D6

TST	PINTST	P31
TEL-CONN	tel-con_simple	K3 K4 K5
JUMPER	LEDV	JP1
DC20-09	DC20-09	K2
DB9	DB9-freestand	J1 J2 J3
HE10-26	he10-26c	P23
FOX-BOARD_J7	foxboard-40pin	P15
FOX-BOARD_J6	foxboard-40pin	P14
FLEX_40	Molex-40pin	P13
CONN-POW	tel-con_simple	K1
CONN_6	SIL-6	P9 P10 P11
CONN_5	SIL-5	P3 P4 P5 P6 P7 P8
CONN_20X2	he10-40c	P2
CONN_20	FSI20-upsidedown	P25 P27
CONN_20	CONN20_SMD	P24 P26 P28 P29 P30 P32
CONN_1	PINTST	P33 P34 P35 P36 P37 P38 P39 P40 P41
CONN_12	SIL-12	P22

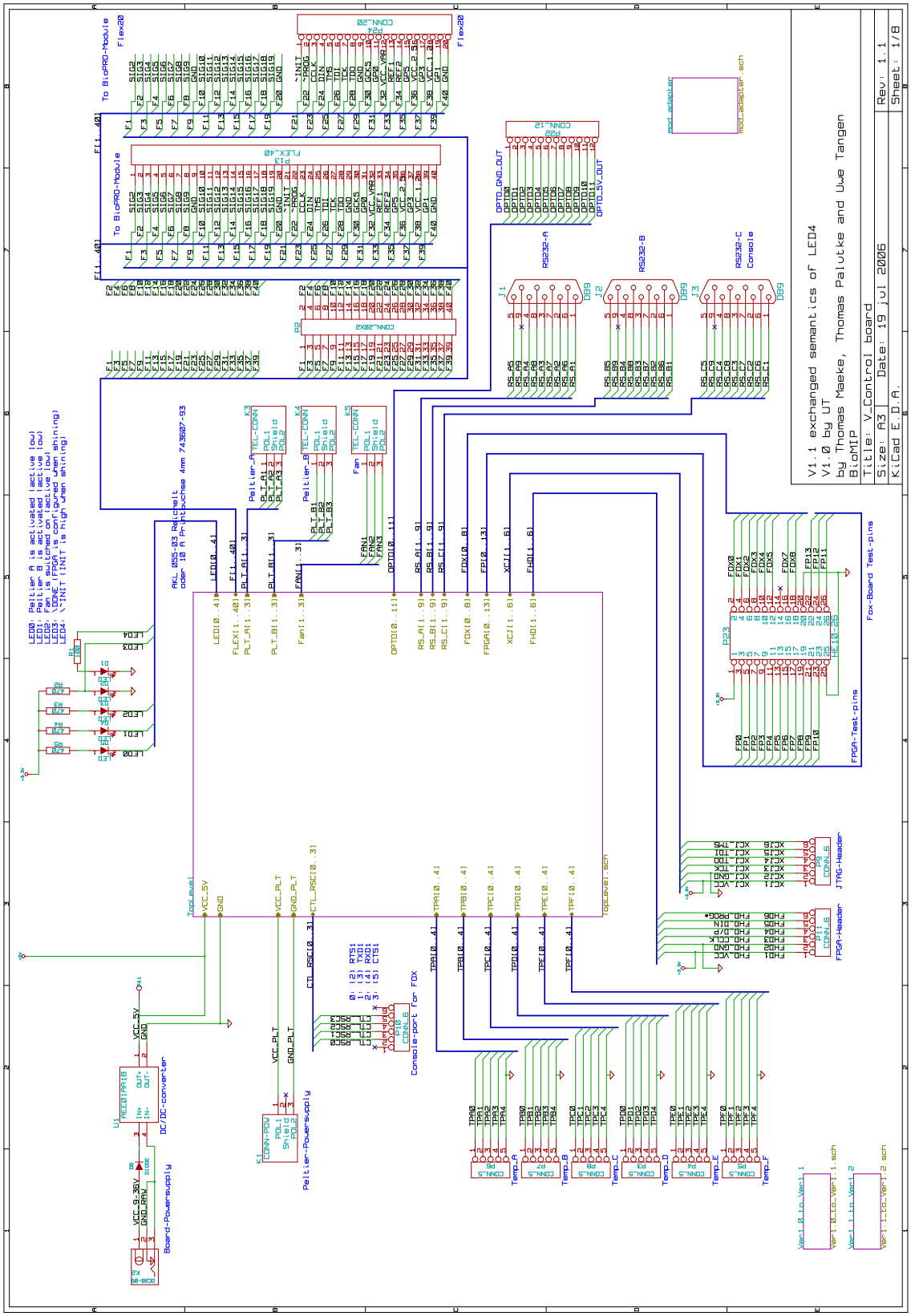
4,7K	SU1206_v	R56
4,7K	SM0805_v	R18 R19 R36 R37 R38 R39 R40 R41 R42 R43 R44 R46 R47 R69 R70 R71
47K	SM0805_v	R12 R13 R14 R68
470	SU1206_v	R24
470	SM0805_v	R2 R3 R4 R5 R11 R27 R28 R29
3,3K	SU1206_v	R50
330	SM0805_v	R67
270	SU1206_v	R23 R26 R52
270	SM0805_v	R30 R31 R32 R33 R34 R35 R45
240	SU1206_v	R20 R21 R22
220	SM0805_v	R66
1K	R3	R9
1K	SU1206_v	R8 R25
1,2K	SU1206_v	R51
10	SM0805_v	R48 R49
100	SM0805_v	R1 R53 R54 R55 R57 R58 R59 R60 R61 R62 R63 R64 R65

220uF	C5V10	C40 C41 C42 C61
47uF	SM1210L_v	C43 C44 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C58 C59 C60 C70 C71
4,7uF	SM1210L_v	C38 C39
100nF	SM0805_v	C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C55 C56 C57 C62 C63 C65 C66

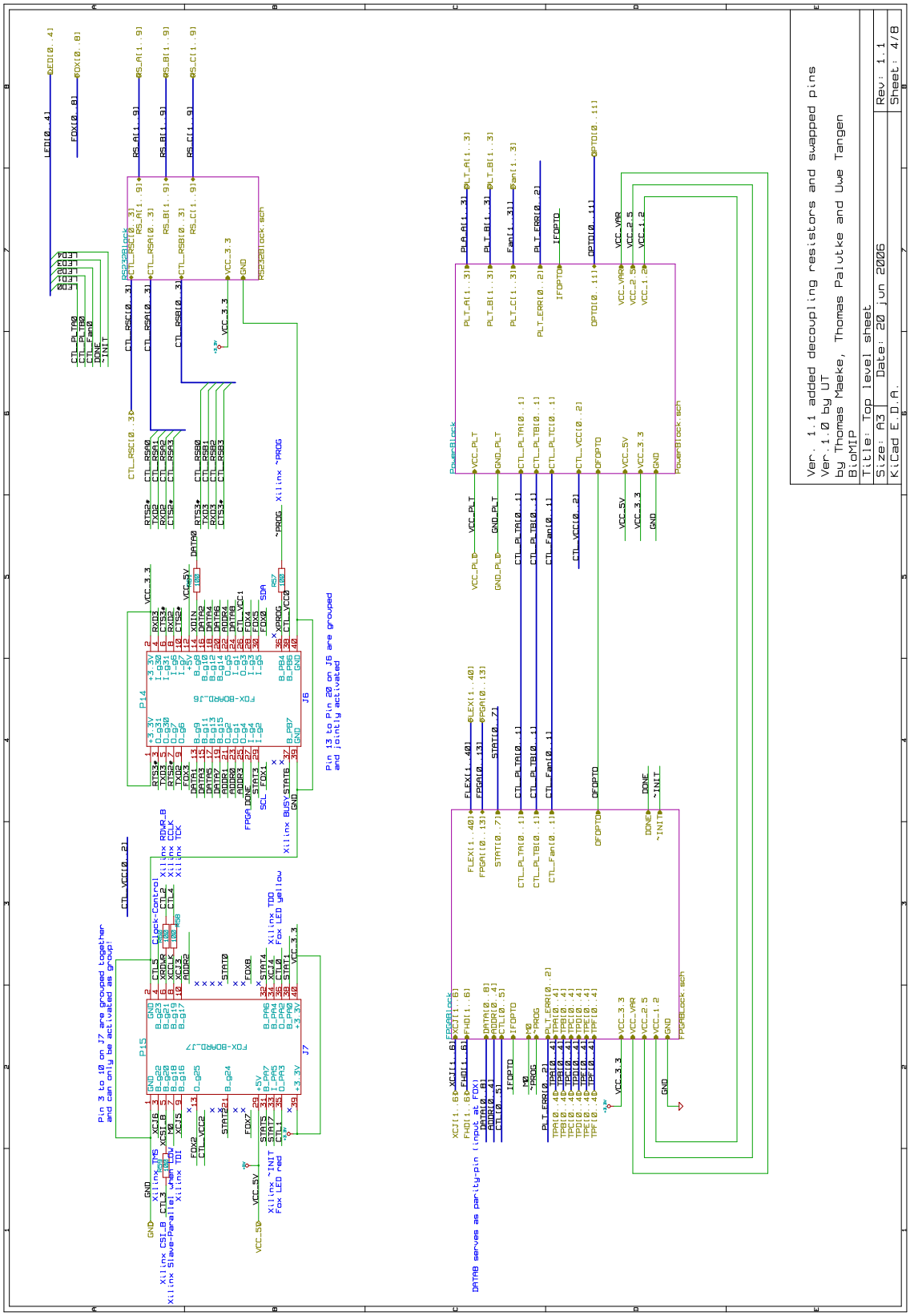
2.2.1 Case connectors

2.3 Schematics

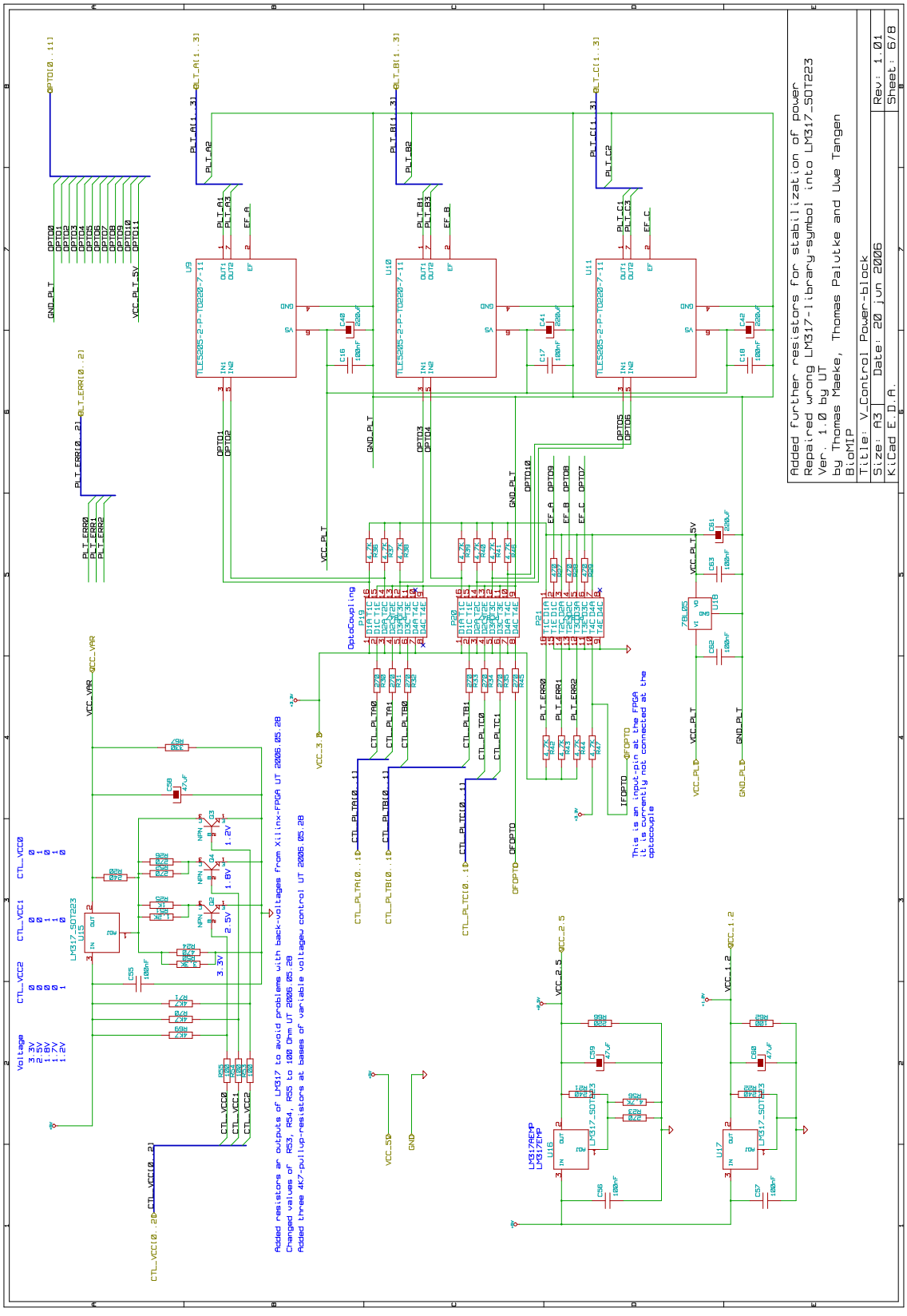
2.3.1 Toplevel



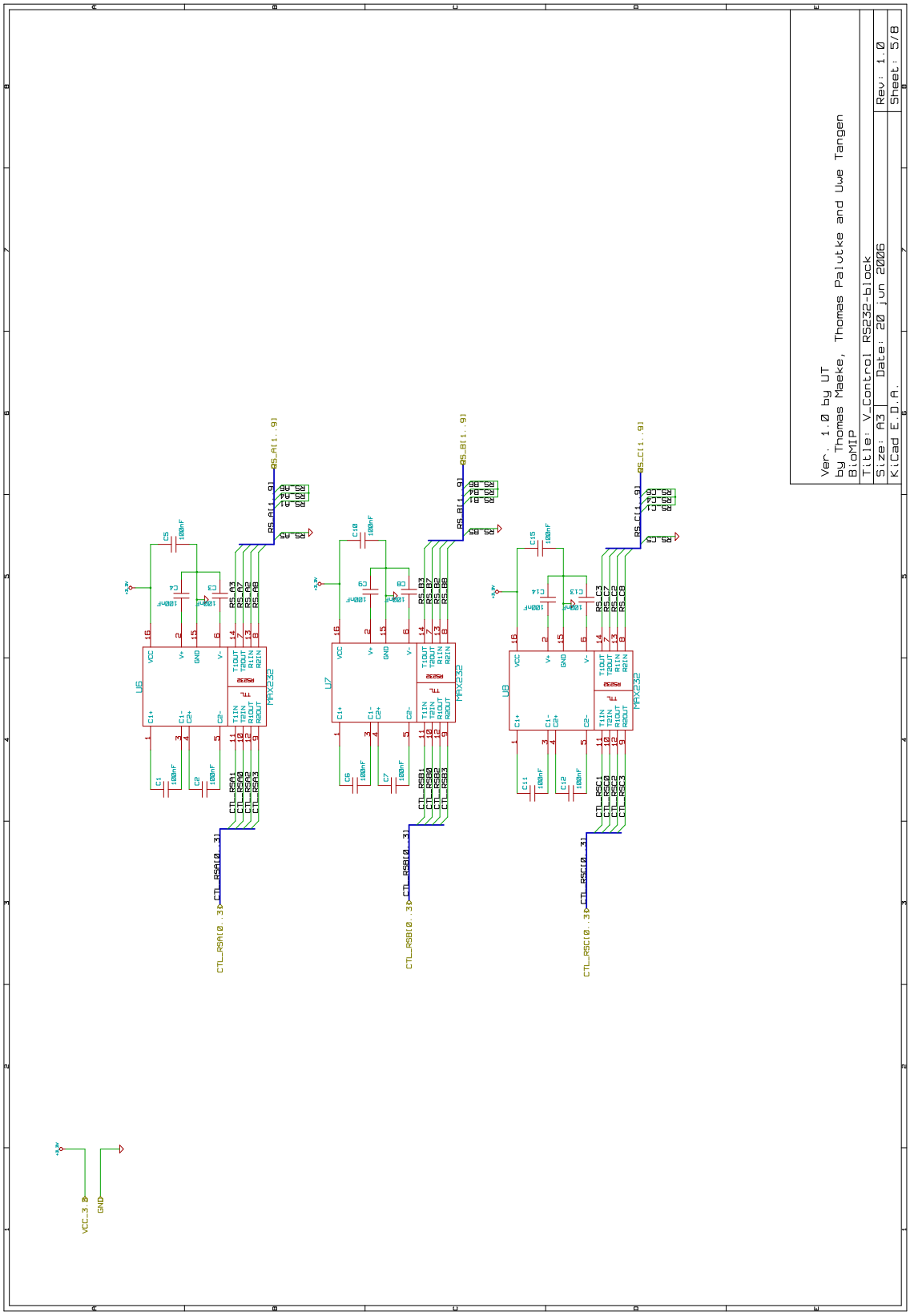
2.3.2 Foxboardconnection



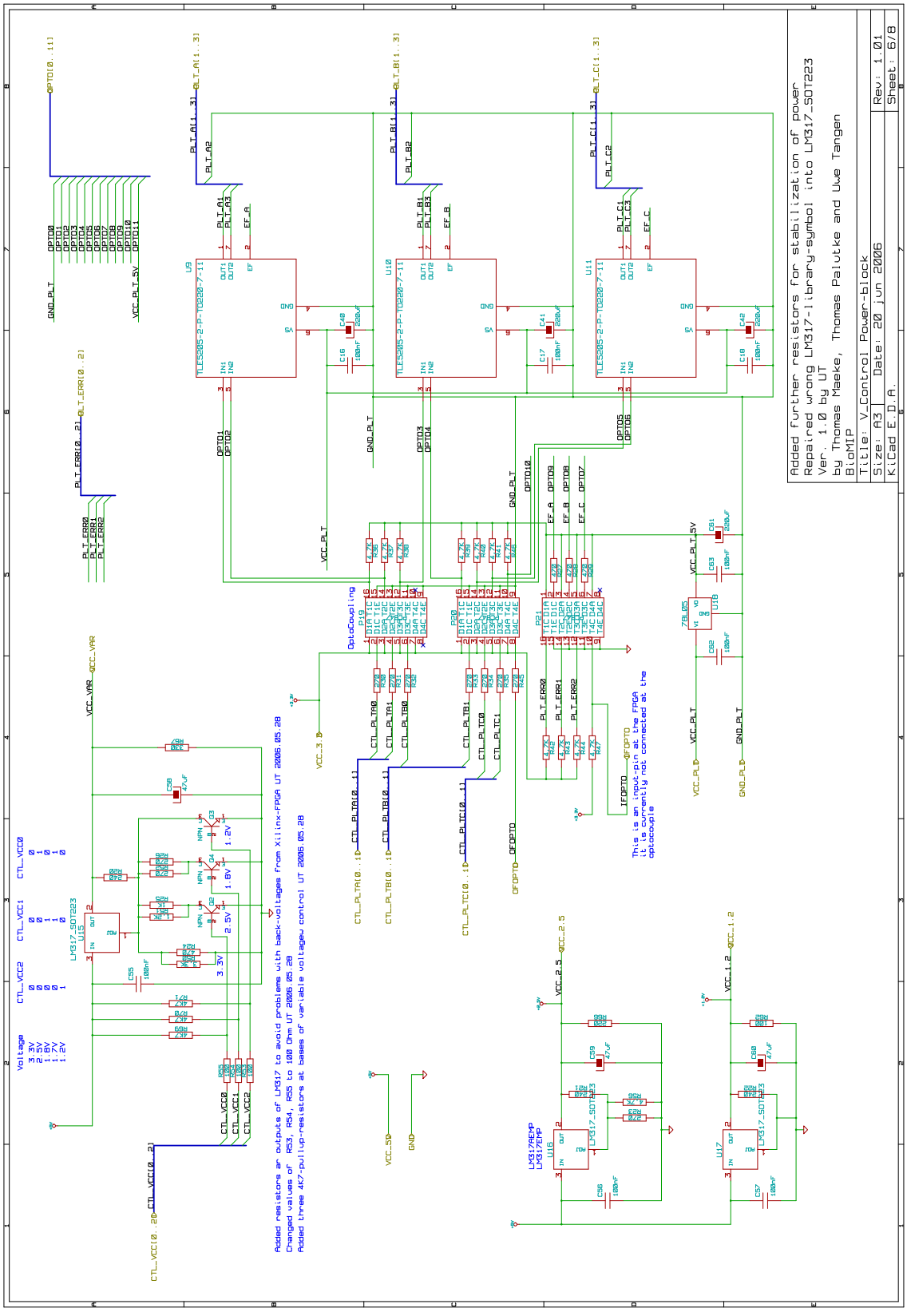
2.3.3 FPGA Block



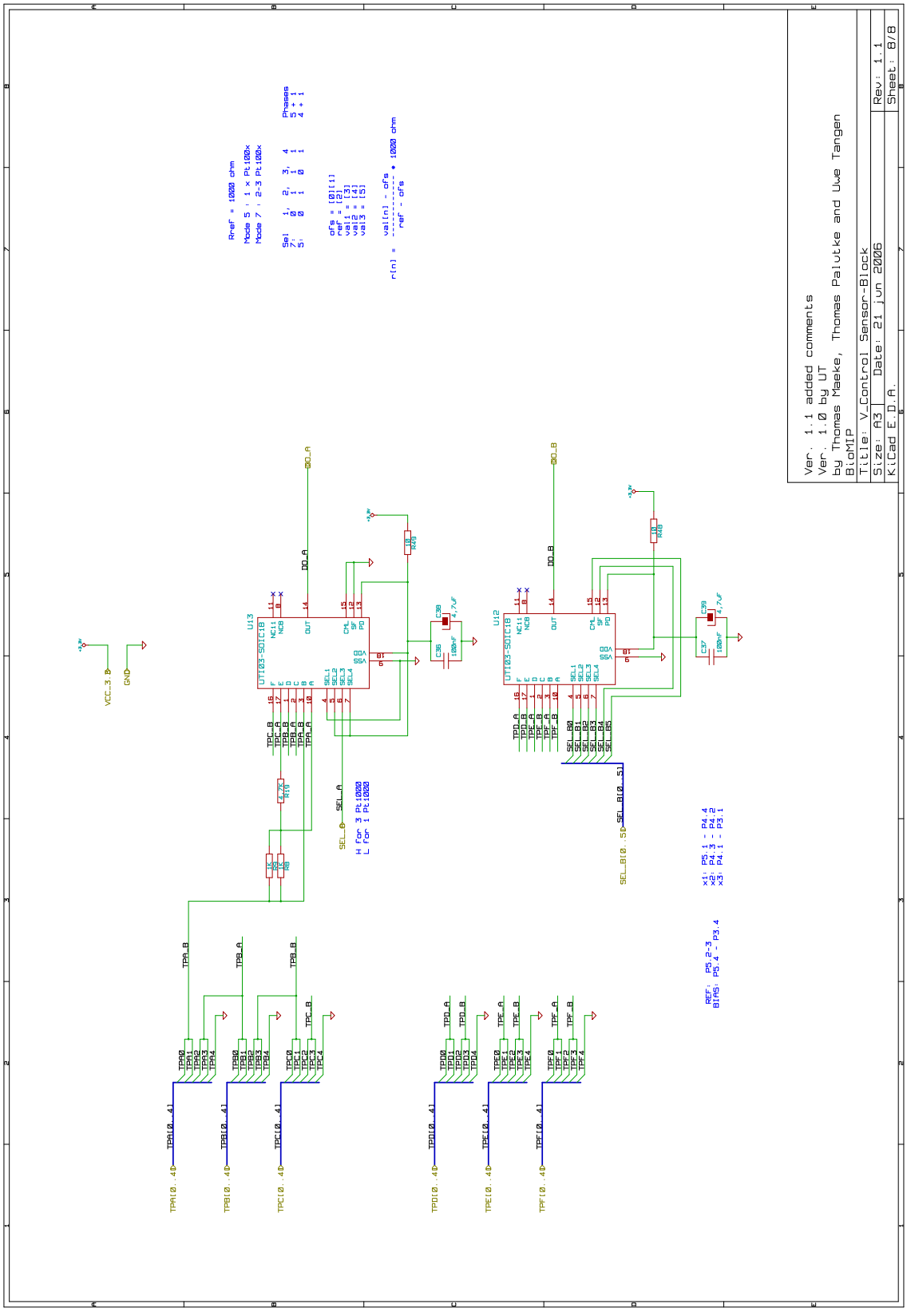
2.3.4 RS-232 Block



2.3.5 Power Block



2.3.6 Sensor Block



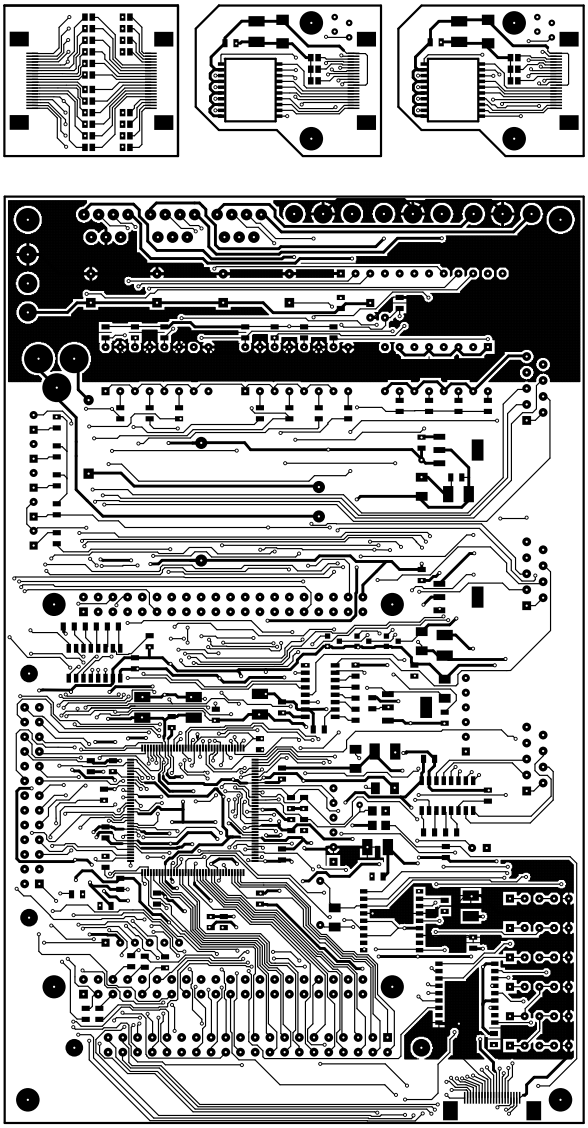
2.3.7 Changes

2006.05.28 Added pullup-resistors to basis of VCC_var-converter
2006.05.28 Removed serial-resistor R57 from DONE-LED because DONE is no longer CLK-ctrl
2006.06.12 Changed meaning of ~INIT-LED which now is shining when INIT is high and added serial resistor of 100 ohm
2006.06.12 Added jumper JP1 to allow JTAG-mode-configuration of FPGA
2006.06.14 Updated pin-layout of TO220-package to allow top-mounting of H-bridges (pin meaning has been swapped 1->7 ..)
2006.06.14 Added load-resistor to DC/DC-converters to alleviate problems with Xilinx-power-train-coupling
2006.06.14 Put DONE-pin at Fox-board-J6-pin-27
2006.06.14 Added CLK-Ctrl of oscillator to FOX-board-J7-pin-4-CTL5 and removed it from DONE-pin at FPGA
2006.06.14 Moved VCC-var-control from FPGA to FOX-board (J6-pin-38, J6-pin-26, J7-pin-15)
2006.06.14 Moved PLT_Err from FOX-board (J6-pin-27, J6-pin-28, J6-pin-30) to FPGA (pin 87, 88, 91)
2006.06.14 Added test-pin for board-clock
2006.06.14 Moved Flex30 and Flex31 (FPGA-pin-128 and pin-129) wires to I/O-pins at the FPGA-pin-125 and pin-126
2006.06.14 Removed CTL[5] net because of pin-limitations
2006.06.14 Moved CSI_B wire from FOX-board CTL[0] to FOX-board CTL[3] because of blockwise enable of outputs.
2006.06.14 Exchanged ~PROG with M0 at FOX-board connector because of blockwise enable of pins
2006.06.14 Added serial-resistors between 3.3V and 2.5V inputs during loading to avoid high-currents due to shunt diodes
2006.06.14 Moved FOX2-net from FOX-J6-pin-38 to FOX-J7-pin-13
2006.06.14 Moved FOX5-net from FOX-J7-pin-15 to FOX-J6-pin-30
2006.06.14 Removed FOX6-net because of pin-limitations of FOX-board
2006.06.14 Moved ADDR2 from FOX-J6-pin-26 to FOX-J7-pin-12 because of routing-problems
2006.06.14 Updated package SOIC18-WIDE to reflect UTI-package
2006.06.14 added a pullup-resistor to CLK_ctrl
2006.06.14 Added a shunt-diode on adapter board to avoid false polarity connections
2006.06.14 Added connection-bridges at adapter voltage-supply to allow different fixed voltage levels.
2006.06.14 Added a new cross-link-adapter instead of one of the former adapters
2006.06.18 Exchanged +3.3V-output at Flex20-connector with VCC_var to allow variable outputs with Spartan 3E FPGAs on Biomodules
2006.06.20 Added +5V-test-pin
2006.06.21 Fixed a bug concerning the pin-name of the LM317 regulators (exchange pin 1 and 3)

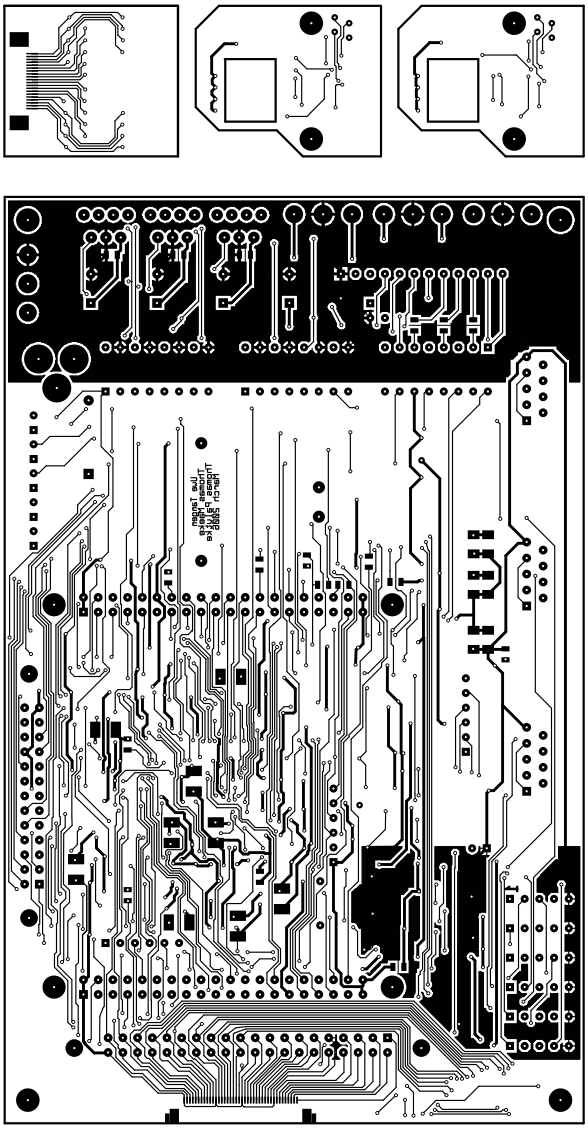
Ver1.1
BioMIP
Title: Changes from Version 1.0 to Version 1.1
Size: A3 Date: 21 jun 2006 Rev: V1.1
KiCad E.D.A. Sheet: 2/8

2.4 Layouts

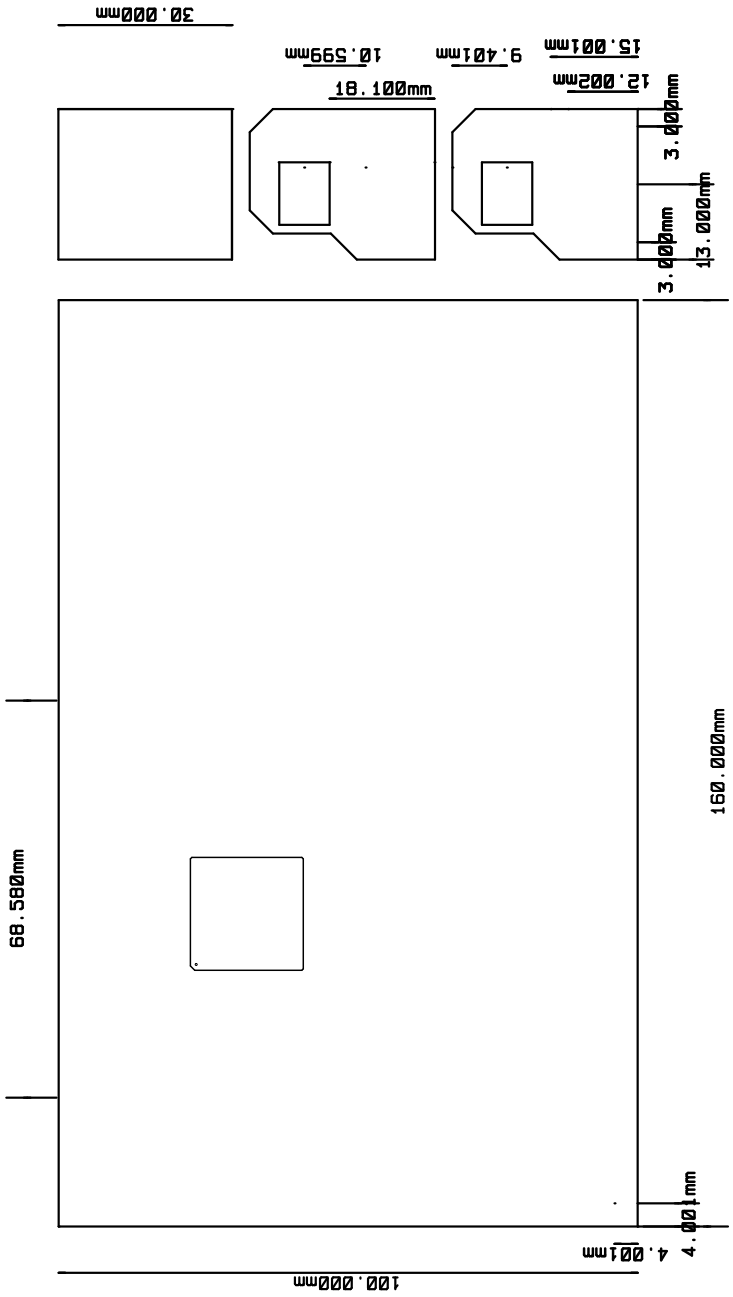
2.4.1 Top



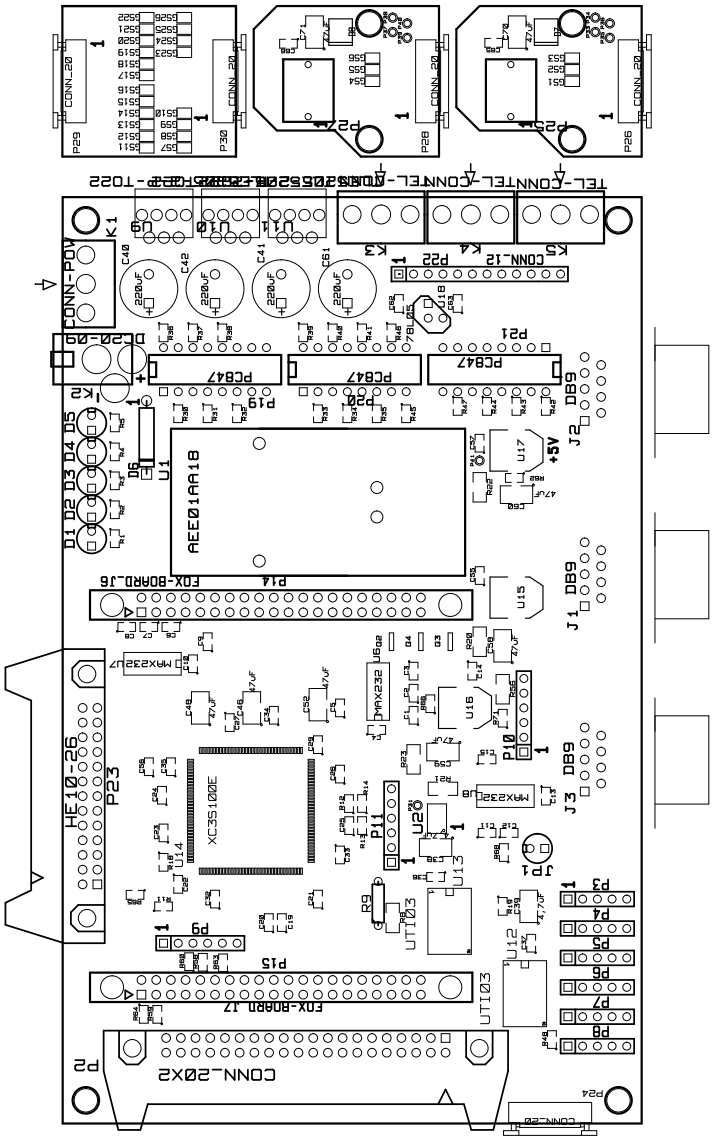
2.4.2 Bottom



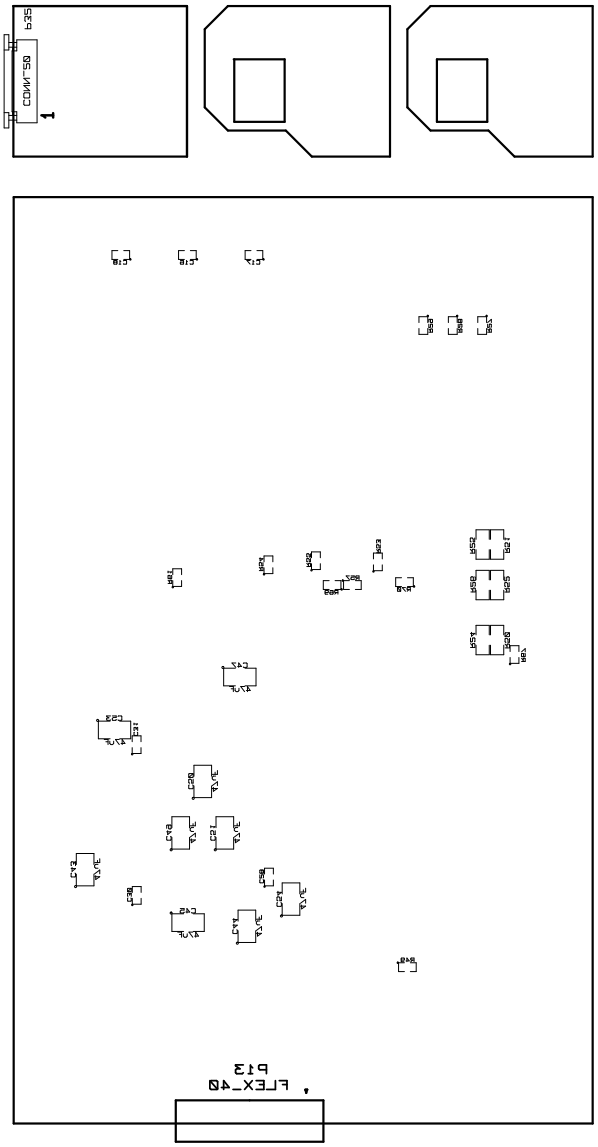
2.4.3 Drawings



2.4.4 Component top

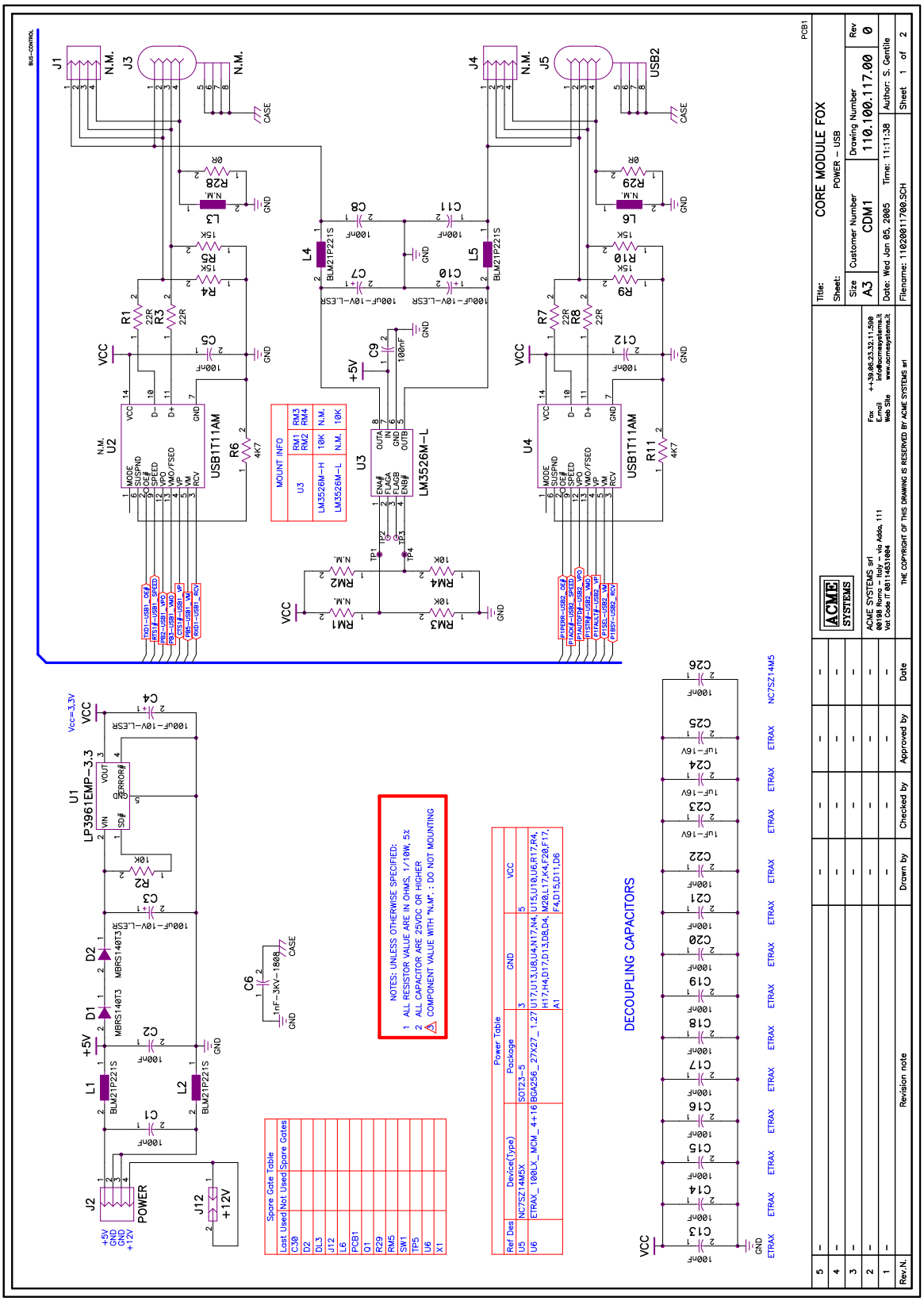


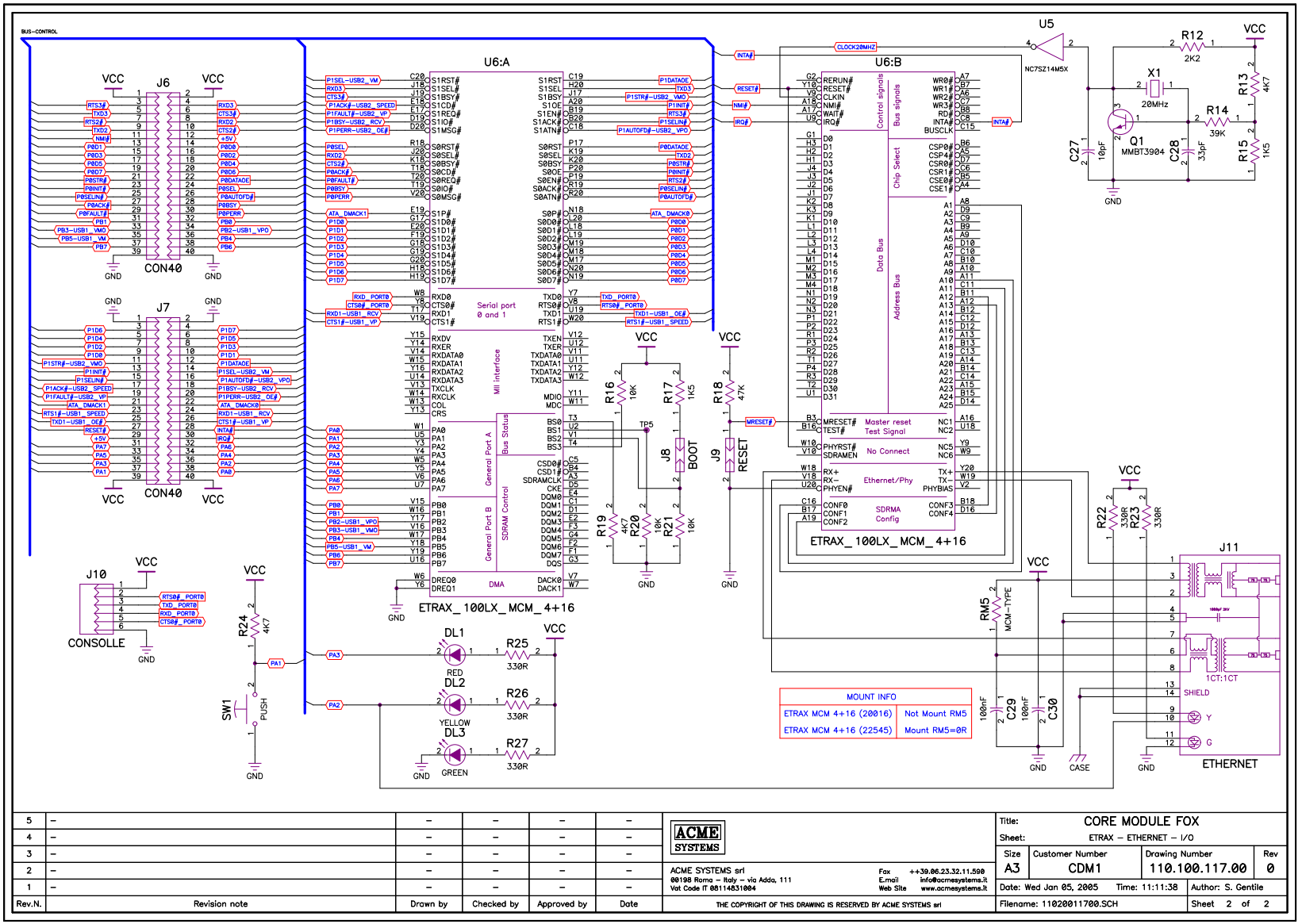
2.4.5 Component bottom



2.5 Foxboard

2.5.1 Schematics





Rev.N.	Revision note	Drawn by	Checked by	Approved by	Date
5	-	-	-	-	-
4	-	-	-	-	-
3	-	-	-	-	-
2	-	-	-	-	-
1	-	-	-	-	-

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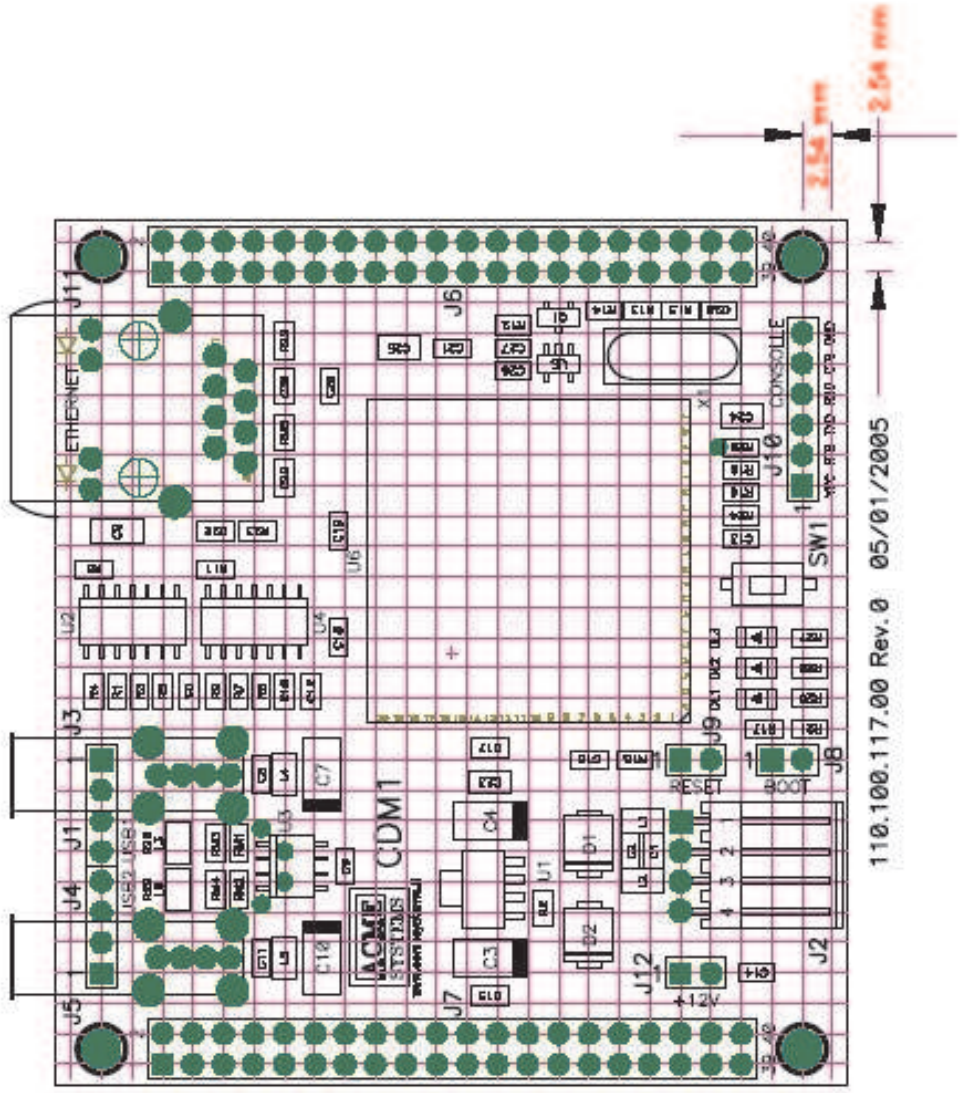
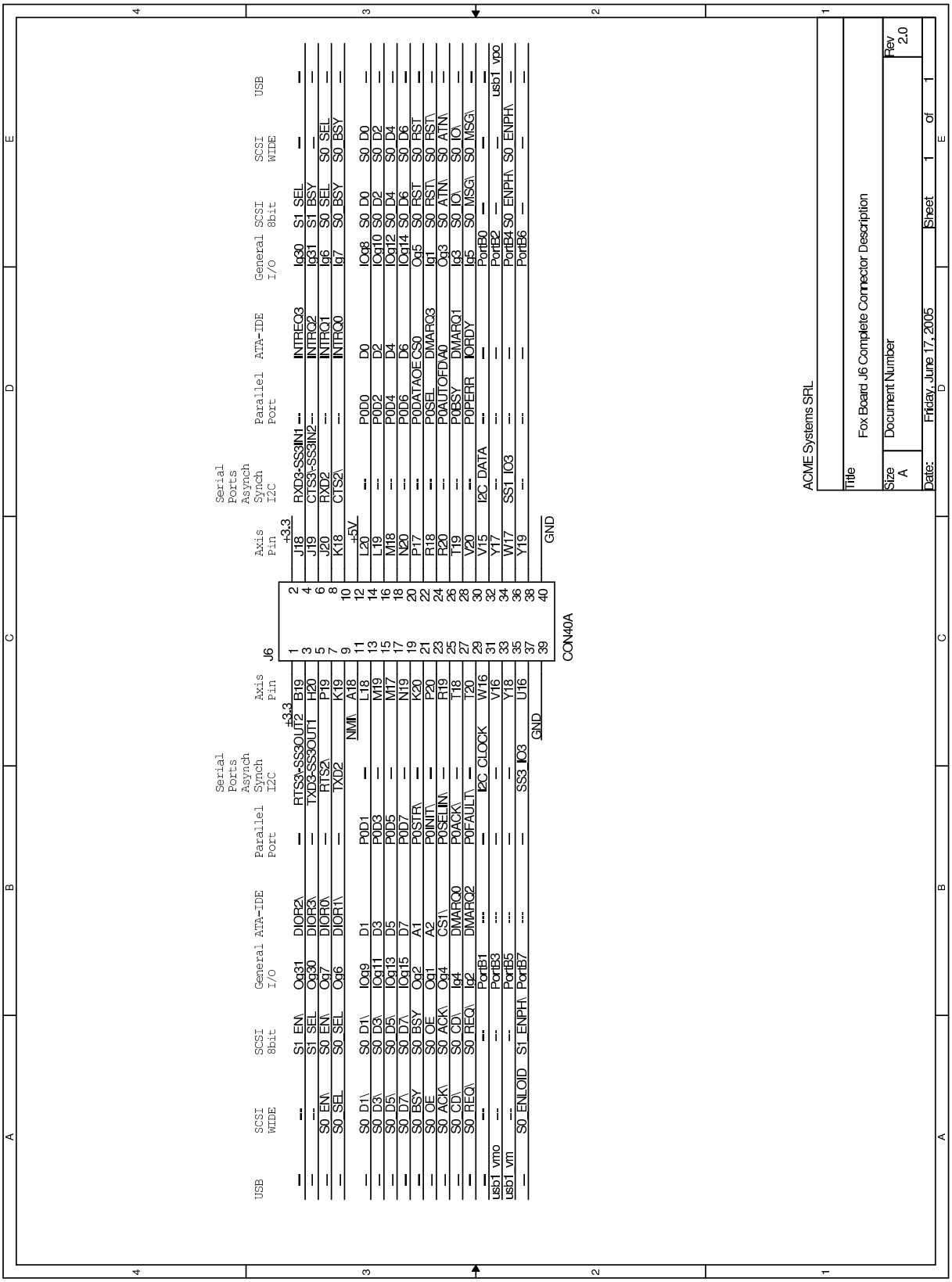
Title:	CORE MODULE FOX
Sheet:	ETRAX – ETHERNET – I/O
Size	A3
Customer Number	CDM1
Drawing Number	110.100.117.00
Rev	0
Date:	Wed Jan 05, 2005
Time:	11:11:38
Author:	S. Gentile
Filename:	110200117 00.SCH
Sheet	2 of 2

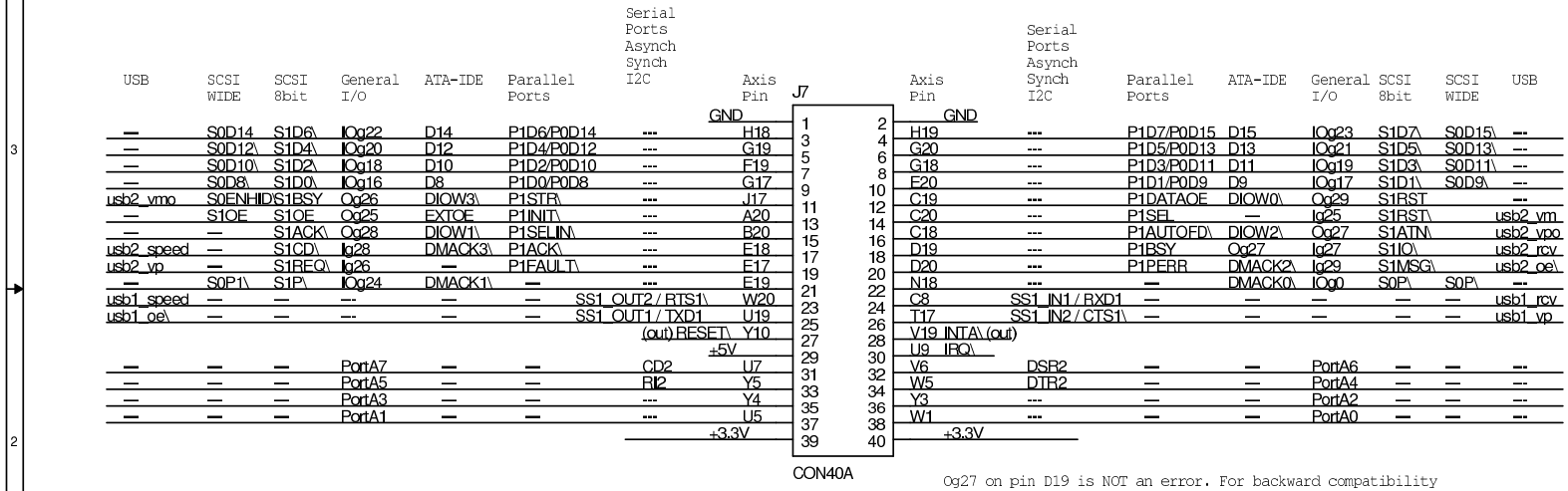
2.5.2 Drawing



Fox mechanical drawing.

2.5.3 Connectors




USB
SCSI WIDE
SCSI 8bit
General I/O
ATA-IDE
Parallel Ports
Serial Ports Asynch Synch I2C
Axis Pin
J7
GND
S0D14 S1D6\ IOg22 D14 P1D6/P0D14 --- H18
S0D12\ S1D4\ IOg20 D12 P1D4/P0D12 --- G19
S0D10\ S1D2\ IOg18 D10 P1D2/P0D10 --- F19
S0D8\ S1D0\ IOg16 D8 P1D0/P0D8 --- G17
usb2_vmo S0ENHIDS1BSY Og26 DIOW3\ P1STR\ --- J17
S1OE S1OE Og25 EXTOE P1INIT\ --- A20
S1ACK\ Og28 DIOW1\ P1SELIN\ --- B20
usb2_speed S1CD\ Ig28 DMACK3\ P1ACK\ --- E18
usb2_vp S1REQ\ Ig26 P1FAULT\ --- E17
S0P1\ S1P\ IOg24 DMACK1\ --- E19
usb1_speed SS1_OUT2 / RTS1\ W20
usb1_oe\ SS1_OUT1 / TXD1 U19
(out) RESET\ Y10
+5V
PortA7 CD2 U7
PortA5 RI2 Y5
PortA3 --- Y4
PortA1 --- U5
+3.3V
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40
CON40A
GND H19 --- P1D7/P0D15 D15 IOg23 S1D7\ S0D15\ ---
G20 --- P1D5/P0D13 D13 IOg21 S1D5\ S0D13\ ---
G18 --- P1D3/P0D11 D11 IOg19 S1D3\ S0D11\ ---
E20 --- P1D1/P0D9 D9 IOg17 S1D1\ S0D9\ ---
C19 --- P1DATAOE DIOW0\ Og29 S1RST usb2_vm
C20 --- P1SEL — Ig25 S1RST\ usb2_vpo
C18 --- P1AUTOFD\ DIOW2\ Og27 S1ATN\ usb2_rcv
D19 --- P1BSY Og27 Ig27 S1IO\ usb2_oe\
D20 --- P1PERR DMACK2\ Ig29 S1MSG\
N18 --- — DMACK0\ IOg0 S0P\ S0P\ ---
C8 SS1_IN1 / RXD1 — — — — — usb1_rcv
T17 SS1_IN2 / CTS1\ — — — — — usb1_vp
V19 INTA\ (out)
U9 IRQ\
V6 DSR2 — — PortA6 — — ---
W5 DTR2 — — PortA4 — — ---
Y3 --- — — PortA2 — — ---
W1 --- — — PortA0 — — ---
+3.3V
Axis Pin
Serial Ports Asynch Synch I2C
Parallel Ports
ATA-IDE
General I/O
SCSI 8bit
SCSI WIDE
USB
Og27 on pin D19 is NOT an error. For backward compatibility when ATA-IDE peripheral is selected, pin D19 is switched to Og27 function.
ACME Systems SRL
Title
Fox Board J7 Complete Connector Description
Size A
Document Number
Rev 2.0
Date: Friday, June 24, 2005
Sheet 1 of 1

Chapter 3

Software/Firmware

3.1 Foxboard

For Foxboard development issues see: www.acmesystems.it `http://www.acmesystems.it/?id=14`

3.1.1 Devicedriver

see:
- etraxgpio.h
- gpio_vc11.c

3.1.2 Programmers API

see:
- vcontrol1_v.h (this is derived from vcontrol.v, see 3.2)
- fox_io.c fox_io.h
- bio_xcs.c bio_xcs.h
- xcs_acc.c xcs_acc.h
- fpga_file.c fpga_file.h
- vc_fpga.c vc_fpga.h
- vc_fpga_func.c vc_fpga_func.h
- vc_xyf.c vc_xyf.h
- ng_xcs_vc.c ng_xcs_vc.h

3.1.2.1 ProScan driver

3.1.2.2 MMT pump driver

3.1.2.3 Temperature/PWM driver

units

3.1.2.4 I2C driver

3.1.2.5 Microfluidic chip driver

3.1.2.6 Z-stage trigger driver

3.1.2.7 Camera sync

3.1.3 Tools

make fox
- create_mpeg

3.2 FPGA

For FPGA programming see: XILINX `www.xilinx.com`

see:

vcontrol1.v
i2c.v

3.2.1 Constraints

see:
vcontrol1.ucf

3.2.2 Tools

make vcontrol fpga

Bibliography

www.xilinx.com
www.acmesystems.it
www.linux.org
andor proscan xyf, camera
mmt pump
pi.com z-stage
tle5204, infineon
uti03, smartec
max232, maxim
lm317, national semi
dc/dc ??
Flex, Molex